High Voltage Gain Single Stage DC-DC Converter Based on Three-State Commutation Cell

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***Abstract*—This paper presents a high voltage gain single stage DC-DC converter based on the three-state commutation cell. The presented converter operates with soft-switching ZVS mode for all switches. The operation principle, project specifications, and experimental results from a 500W prototype are presented in order to validate the proposed structure. The results show de soft switch commutation, reduced stress and high efficiency (over 94%).**

I. INTRODUCTION

Several applications, as UPS and motor drives, commonly need to step and input voltage up, normally between 12V and 125V, provided from batteries and PV panels, to produce a DC bus of 200V~400V, to feed the inverters [1]. In this aspect, the conventional boost converter is not suitable, as the high duty cycle used would lead it to instability. An alternative is to use cascaded boost converters, but this solution leads to low efficiency due to the high number of energy processing stages [2]. Thus, in order to overcome these disadvantages, some high voltage gain boost converters were developed, as in [3-5].

Looking for a better efficiency and simplicity, some recent structures focus the reduction of conversion stages, as can be observed in [6-9]. Thus, this paper presents the study and the physical implementation of a high voltage gain boost converter, based on the three-state commutation cell, for battery charging and to produce a 200V DC bus in a single conversion stage, using PV panels. The system presents the following specifications: input voltage of 24V, switching frequency of 50kHz, output voltage of 200V, and load power of 500W. On figure 1, it can be observed the circuit schematic of the proposed topology.

This paper presents a new high voltage gain DC/DC converter, as can be seen in Figure 1. The main advantage of the proposed structure is the low voltage stress across the switches, which is naturally achieved by the converter characteristic, without the need of inserting an extra auxiliary circuit for achieving ZVS operation. A single-stage converter with high step-up gain then results, while an integrated system with battery charging from a photovoltaic panel is also obtained. The duty cycle allows the MPPT control and the battery absorbs or delivery energy automatically according to the load condition and maintaining acceptable output voltage regulation.

II. CONCEPTION OF TOPOLOGY

The bidirectional characteristic of the topology allows either charging the battery from the PV array or feeding VDC3. Besides, the use of resonant capacitors in the full-bridge capacitors allows soft switching (ZVS) of the switches. The integrated topology resulting from the boost full bridge and three state switching cell is shown in Fig. 1. The main advantage of this topology is the low voltage stress across the active switches, low input current ripple and simplicity, what results in higher efficiency [10-12].

Some high voltage gain topologies have three dc links as shown in Fig. 2, where VDC3 feeds the inverter with a higher voltage than that of the remaining ones. According to the proposal, the battery bank and the photovoltaic panel can be connected to the low voltage VDC1 or VDC2, depending on the available voltage levels. Considering typical applications under 2kW, battery banks voltage levels can be 12V, 24V or 48V (in order to avoid the connection of many units in series) and photovoltaic panels can be arranged to establish a dc link with voltage level equal to about twice that of the former link.

III. OPERATION PRINCIPLE

The presented converter has two operation regions, which work both similarly. The duty cycle is applied on the lower switches of each leg (S2 and S4), which operate in opposite phase. The converter behavior and the operation region are defined by the applied duty cycle. If the duty cycle is higher than 50%, the lower switches work in superposition, and if the duty cycle is lower than 50%, then only the upper switches are superposed.

The converter presents six operation stages. The proposed topology is formed by the an input inductor L_{IN}, four controlled power switches S1-S4, two rectifier diodes D1 and D2, two three-state commutation cells T1 and T2, two transformers Tr1 and Tr2, and four output capacitors C1-C4. Figure 2 presents the theoretical waveforms. On the final version, it will also be presented the detailed description of each operation stage and characteristic equations.

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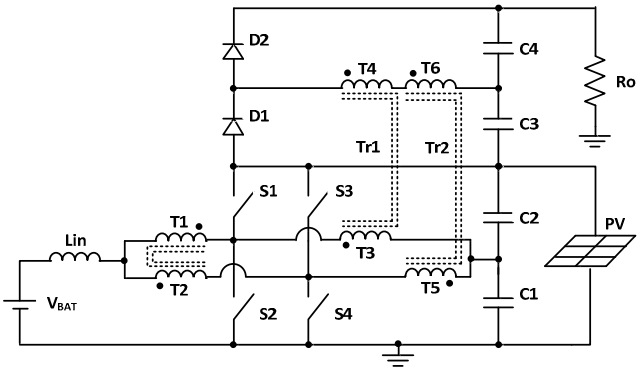

Figure 1. Proposed topology using a PV system.

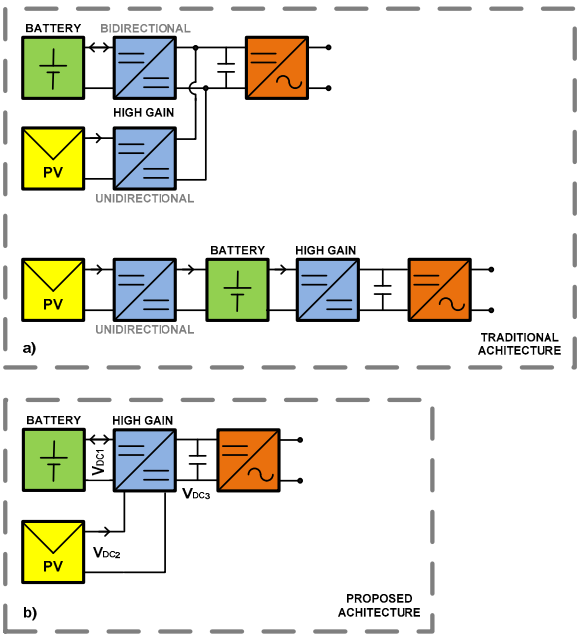

Figure 2. a) Conventional Architecture b) Proposed Architecture

As can be observed, the current through the input inductor has a frequency two times higher than the switching frequency, which characterizes the three-state commutation cell behavior. This current is then equally divided between the cell autotransformers, which leads to reduced current stresses. The windings T3 and T5 correspond to the transformer primary side, which are responsible for both step the voltage up, and to allow the switches to operate in ZVS conduction mode, increasing the system efficiency.

First Stage [$t_0 - t_1$] - This stage begins when S1 turns-off, causing a current flow through the anti-parallel diode of switch S2, allowing its turning-on in ZVS. At this moment, S3 was turned-off, and S4 turned-on. The current flowing through the input inductor 'I_{IN}' increases linearly and is equally divided between the two switching cells, reducing the associated stresses of the active semiconductors. The current on the primary side T3 decreases linearly, while the current through T5 increases linearly. This stage ends when the currents in T3 and T5 reach zero, and the current through S2 is equal to the one through S4.

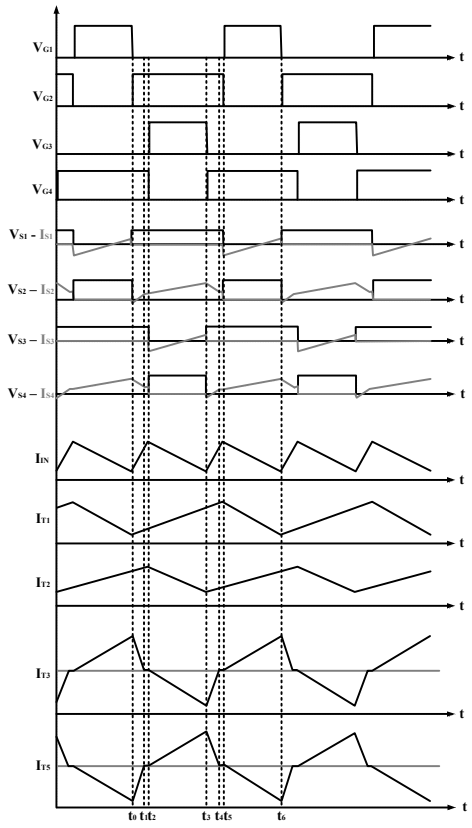

Figure 3. Main theoretical waveforms.

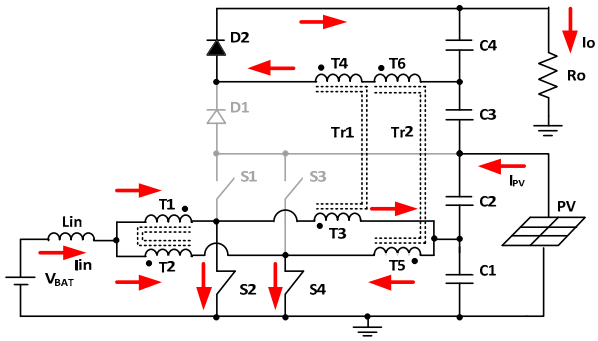

Figure 4. First Stage.

Second Stage [$t_1 - t_2$] – At this stage, 'I_{IN}' is still linearly increasing and is equally divided through the commutation cells. Also, all the rectifier diodes are reversely polarized. The current through T3 and T5 remain null. This stage ends when S4 turns-off.

Third Stage [$t_2 - t_3$] – This stage begins when S4 turns-off, causing a current flow through the anti-parallel diode of S3, allowing its turn-on in ZVS mode. At this moment, S2 was already turned-off. The current flowing through the input inductor 'I_{IN}' decreases linearly, while the current through T1 remains increasing linearly, and decreasing linearly in T2. The current on the primary side T3 increases linearly, while the current through T5 decreases linearly. This stage ends when S2 is turned-on.

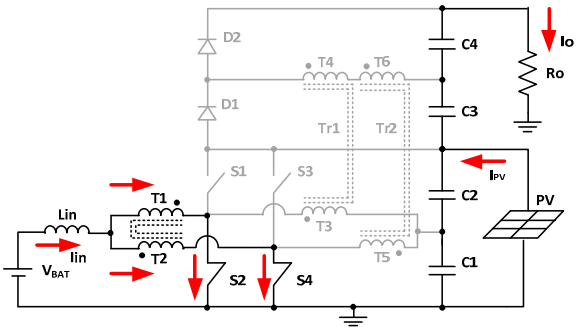

Figure 5. Second Stage.

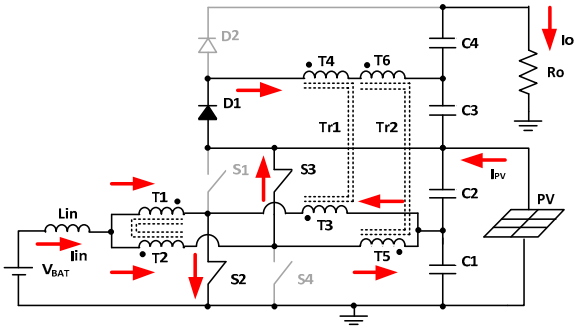

Figure 6. Third Stage.

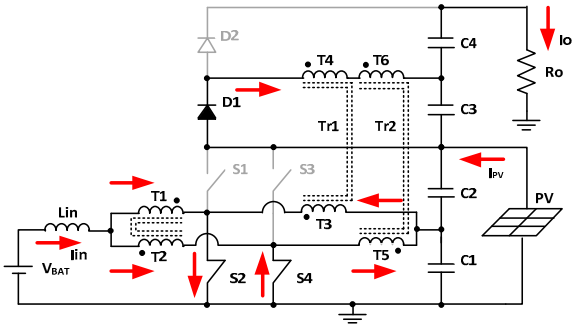

Figure 7. Fourth Stage.

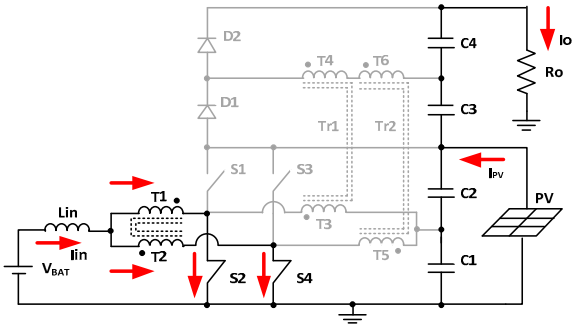

Figure 8. Fifth Stage.

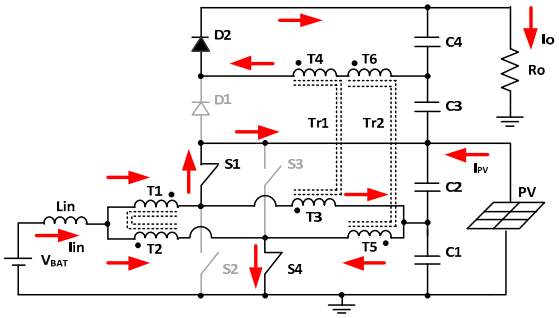

Figure 9. Sixth Stage.

Fourth Stage [$t_3 - t_4$] – This stage begins when S3 turns-off. As S2 is turned-on, the input current 'I_{IN}', and consequently through T1 and T2, increases linearly. Also, the current through S3 increases and has its direction inverted. The current through T3 linearly increases, while the one through T5 decreases. This stage ends when theses currents in T3 and T5 reach zero, and the current through S2 is equal to the one in S4.

Fifth Stage [$t_4 - t_5$] – This stage is similar to the second one. At this stage, 'I_{IN}' is still linearly increasing and is equally divided through the commutation cells. Also, all the rectifier diodes are reversely polarized. The current through T3 and T5 remain null. This stage ends when S2 turns-off.

Sixth Stage [$t_5 - t_6$] – This stage begins when S2 turns-off, causing a current flow through the anti-parallel diode of S1, allowing its turn-on in ZVS mode. At this moment, S3 was already turned-off, and S4 turned-on. The current flowing through the input inductor 'I_{IN}' decreases linearly. The current on the primary side T3 increases linearly, while the current through T5 decreases linearly. This stage ends when these currents through T3 and T5 become null, and the current through S2 is equal to the one through S4. After this stage, there is a new switching cycle, reinitiating from the first stage.

IV. STATIC GAIN

This section presents the graphics used to obtain the converter static gain for two operation regions, as the correspondent equations. From these equations, it can be inferred that the duty cycle depends exclusively on the duty cycle 'D', the transformer voltage relation 'n', and the parameterized load current 'α'. The static gain equations for D>50% and D<50% are presented as follows.

$$G_{D>50\%} = \frac{1}{(1-D)} + \frac{2.n}{\left[(1-D)+\alpha\right]} \quad (1)$$

$$G_{D<50\%} = \frac{1}{(1-D)} \cdot \left[\frac{2.n.D^2}{D^2+\alpha.(1-D)} + 1\right] \quad (2)$$

$$\alpha = \frac{4.n.I_0.L_S}{V_{BAT}.Ts} \quad (3)$$

The parameterized load current 'α' depends on the battery voltage, the load current, the switching period, the transformer relationship, and on the transformer leakage inductance 'LS'.

Figure 10 presents the curves relating the static gain (G) with the duty cycle (D) for different values of (n).

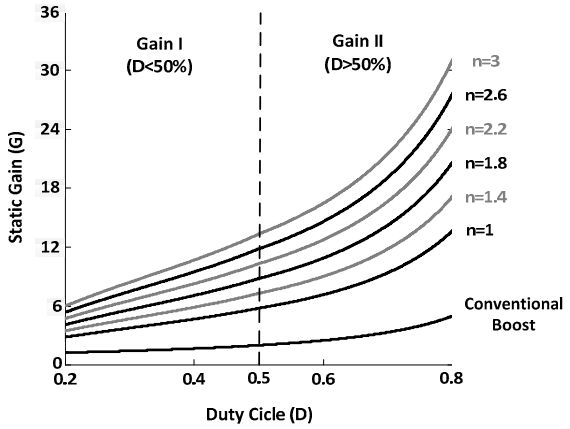

Figure 10. Relation G x D for different values of 'n'.

Figure 11 presents the curves relating the static gain (G) with the parameterized load current (α) for different values of (D).

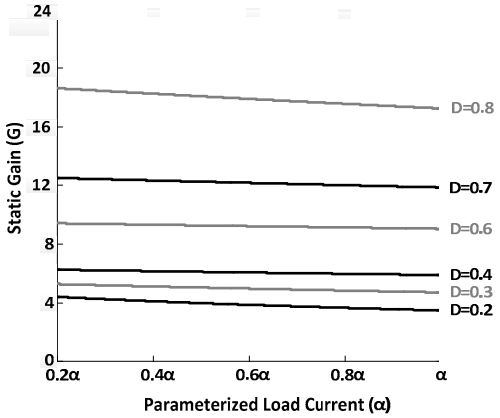

Figure 11. Relation G x α for different values of 'D'.

V. SOFT-SWITCHING CONDITION

This section presents the graphics with the minimum and maximum dead times necessary to obtain soft-switching operation on the switches. Figure 12 shows the upper and lower switches soft-switching condition varying with the parameterized load current for different values of duty cycle. From this figure, it can be observed that the duty cycle variation plays a small role on the commutation condition, in comparison with the commutation duration.

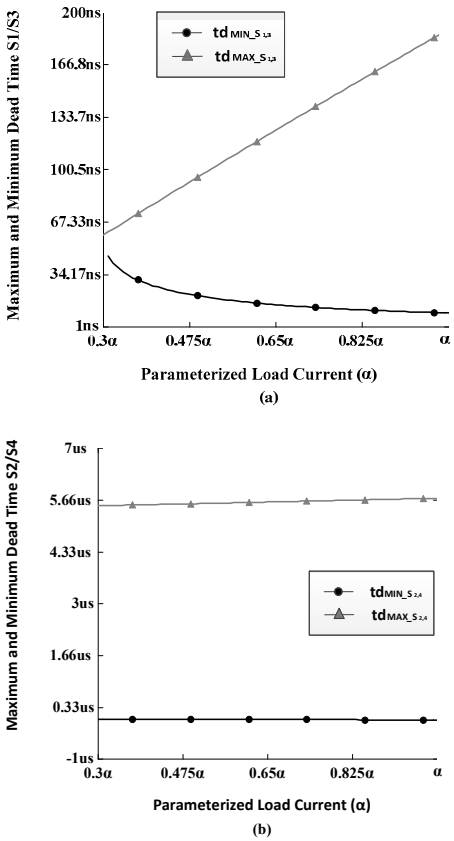

Figure 12. Upper and lower switches soft-switching condition.

VI. EXPERIMENTAL RESULTS

This section presents the experimental results obtained from the converter operating in nominal power condition. Table I shows the prototype project specifications.

TABLE I. PROTOTYPE PROJECT SPECIFICATIONS

Switching frequency	Fs = 50kHz
Input voltage	V_{IN} = 24V
Output voltage	V_{out} = 200V
Load power	P_0 = 500W
Input inductance	L_{IN} = 100uH
Output capacitors	C1, C2, C3 and C4 = 100uF
Transformer relationship on the three-state commutation cell	(1 : 1)
Transformer relationship of Tr1 and Tr2	(1 : 1.4)

Figure 13 presents the voltage waveform across the output capacitors, where it can be noticed that the sum of each of these voltages results in the output voltage.

Figure 14 presents the voltage across the diodes D1 and D2 respectively, where it can be noticed that they both operate complementally, with no overvoltage and clamped in approximately 150V.

Figure 15 presents the current behavior from the input current and through the switching cells, where it can be observed the correct distribution of the current through T1 and T2. In this way, the stresses on the active devices are reduced.

Figure 16 presents the voltage and the current through S1, where it can be noticed the operation in ZVS mode. The switch S3 presents the same behavior, though shifted from 180°. Figure 17 shows the detail from the commutation operation over S1.

Figure 18 presents the voltage and the current through S2, which is complementary to S1. The commutation detail can be observed in Figure 19.

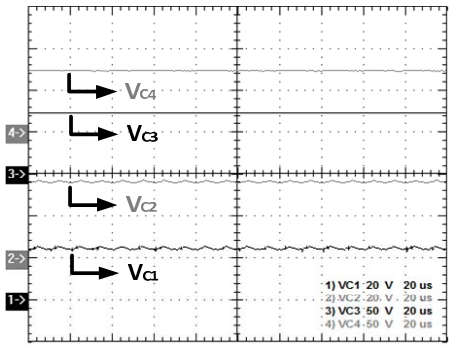

Figure 13. Voltage across the output capacitors.

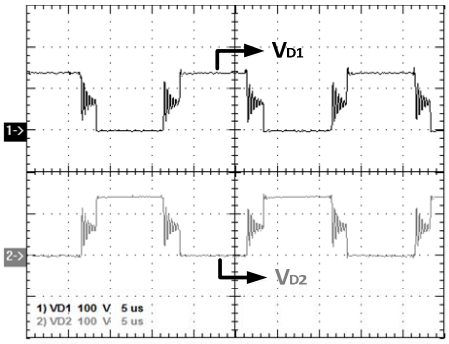

Figure 14. Voltage across D1 and D2.

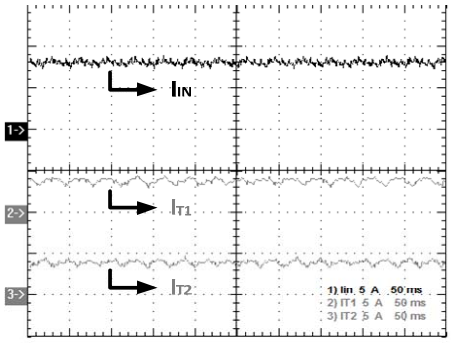

Figure 15. Input current, and through the switching cells.

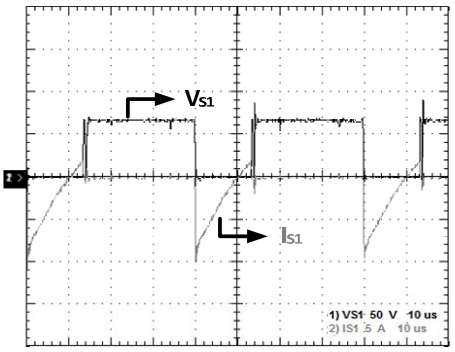

Figure 16. Voltage and current through S1.

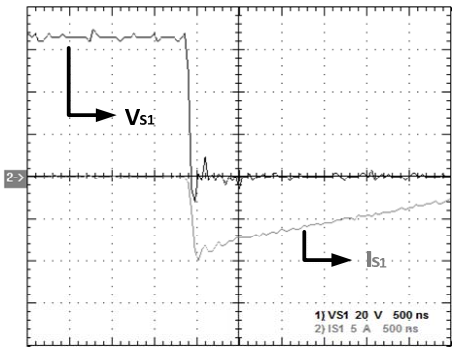

Figure 17. S1 soft-switching detail.

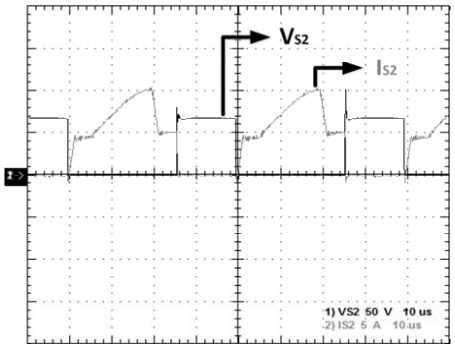

Figure 18. Voltage and current through S2.

Figure 20 presents the efficiency curve relative to the proposed converter, where it can be observed the high efficiency achieved, approximately 94% for nominal load.

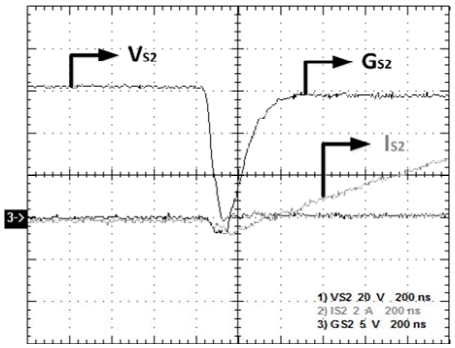

Figure 19. S2 soft-switching detail.

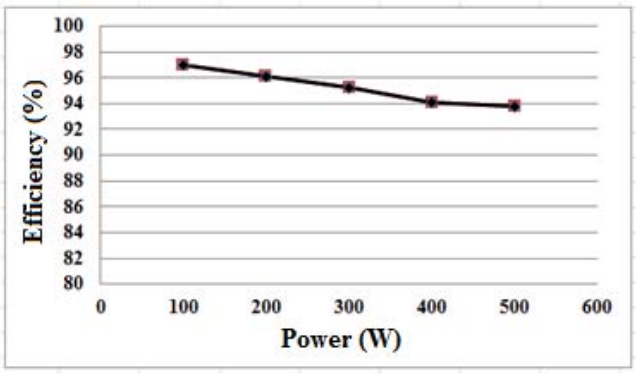

Figure 20. Efficiency curve.

VII. CONCLUSION

A boost converter with high voltage gain was presented, and its equations, operation principle, and main theoretical waveforms were all detailed. The topology presents, as main feature, a large voltage step-up with reduced voltage stress across the main switches, important when employed in grid-connected systems based on battery storage, like renewable energies systems.

Experimental results obtained from a 500W prototype validate the concept, with high efficiency along a wide load range (>94%), and confirming the satisfactory performance of the structures. Thus, the idea of integrating converters in a single stage seems to be promising on the path to obtain additional topologies feasible to photovoltaic and fuel cell applications.

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